Imbedding Ultra-Thin Chips in Polymers
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Abstract—In this paper we describe a technology for embedding ultra-thin chips inside polymers. In this context, the process description and advantages of using two different polymers; one for embedding chips and the other as reinforcement layer on top and bottom of the complete stack would be demonstrated. We also refer to the results from investigations performed to determine the optimum thickness of polymer layers to compensate the inherent warpage resulting from high expansion and shrinkage effect during thermal curing of polymers.

In addition to these, the consequence of inherent warpage effect of ultra-thin chips during embedding process will also be demonstrated. Finally, a delicate process for delamination of embedded chip from the handling substrate will be presented along with challenges and possible solutions to them.

Index Terms—Polymers, Chipfilm™, Polyimide, Flexible electronics, Benzocyclobutene (BCB), Perforated carrier.

I. INTRODUCTION

Flexible electronics technologies presents themselves as promising fields for next generation consumer electronics applications. The first and foremost leap in this challenge is the introduction of ultra-thin chips (thickness <20µm) which, unlike stiff silicon chips, are well bendable and mechanically reliable [1]. The hybrid combination of such ultra-thin chips with large area electronics is defined as Systems-in-Foil (SiF) [2]. Chipfilm™ technology allows for fabrication of very thin chips having a defined chip thickness and featuring high mechanical stability [3]. In the first attempts to use Chipfilm™ technology [1] in flexible electronics applications the ultra-thin chips were glue-attached to a flexible substrate carrier. The piezoresistive effect on different devices and circuits fabricated on ultra-thin chips glued to flexible substrate was investigated by using an in-house bending apparatus [4]. While this setup is suitable for test purposes, practical applications will require imbedding of the ultra-thin chips within the foil substrate for ease of realizing the interconnections and presenting them into industrial production.

In this paper we describe a technology for embedding ultra-thin chips inside polymers. The procedure of two polymer embedding technique; one for embedding the chips and the other as reinforcement layer respectively on top and bottom of the embedded chip, has been described in details. Later, we have elaborated challenges that we faced during the work along with possible solutions to them. We have also described two delicate processes for delamination of embedded chip from the handling substrate. At the end of the paper we have described our future goals to improve the embedding process and the introduction of new processing steps after the successful embedding process.

II. CHIPFILM™ TECHNOLOGY

The conventional production of ultra-thin chips involves the grinding of the entire wafer back to the desired thickness after the circuit integration steps are already carried out. This type of processing may lead to an undesirable yield loss at the very end of the chip production. Also, it can result in non-uniformity of the ultra-thin chip thickness where very precise and accurate control of the thickness is necessary.

In contrast to the subtractive back grinding process, there is an alternative additive process known as Chipfilm™ developed at IMS (Institut für Mikroelektronik Stuttgart), where the final thickness of the ultra-thin chips is defined long before the circuit integration in an additional process step. The main feature of this process is the precise control of the thickness uniformity of the ultra-thin chips produced. Using this unique process, ultra-thin chips of thickness well below 20 µm with extraordinary uniformity all over the chip area becomes feasible.

At the very beginning of Chipfilm™ process fabrication, a two-step selective anodic etching of p-doped bulk silicon is performed which results in a fine porous layer positioned over a course porous silicon layer on the wafer surface. During the following sintering step, the silicon material in the porous layer rearrange itself to convert the course porous layer to big cavities which results in empty spaces in between the fine porous layer and the solid silicon wafer. Subsequently, a silicon epitaxial layer is deposited on the fine-porous (Fig. 1-a). The desired effective thickness of the ultra-thin chips can be determined during this epitaxial layer deposition process and hence can be controlled very precisely. Vertical silicon anchors (Fig. 1-b) spreading all over the cavity area with defined pitch distances among them underneath the chip, keep the chip in place during subsequent circuit integration steps. Also the chips are secured at the edge to the handling wafer. Therefore, the integration of electronic components and circuits on Chipfilm™ can go through the same standard process like bulk wafers. After the circuit integration task is completed, deep tranches through the epitaxial layer are etched...
along the chip edges to reach the cavities. At this stage, the chips are separated from each other and are only attached to the substrate wafer weekly by mean of vertical anchors. By breaking these vertical anchors, the chips can be picked by using a standard pick-tool from the substrate. One import advantage of the Chipfilm™ besides its precise control over chip thickness is that a simple and robust handling throughout the entire manufacturing process is possible with this technology [5].

III. IMBEDDING ULTRA-THIN CHIPS IN POLYMER
For making the ultra-thin chips conformable and usable in flexible electronics technologies, they have to be mounted on flexible substrates. This mounting can be done in two ways; either by attaching the ultra-thin chips to the flexible substrate by means of glue attachment or embedding the ultra-thin chips inside the polymers which will eventually work as flexible substrate for the chips.

The first alternative where the chips are glue attached to the flexible substrate carrier, are more suitable for experimental purpose rather than actual usage into flexible systems. Because the main challenge in this regard is the realization of the electrical contact to the outside. The first attempts to use the Chipfilm™ chips for the flexible electronics application was by gluing the chips on kapton® foils of thickness >50µm. The electrical contacts were realized by means of Aluminum wire bonds. By using an in-house bending apparatus and the glue attached chips on foil we have presented recently that the piezoresistive effect may have an impact on parametric circuit yield [4]. We have also shown that the glue attached chips exhibit an apparently non-linear piezoresistive effect [4]. This non-linearity is believed to be associated with chip warpage which tends to become compensated by the glue attachment while introducing biaxial stress offsets within the active layers [6]. This important packaging related issue will be discussed further in section IV.

Gaining experiences and results from glue mounted chips on flexible substrate we have started engaging into research work for embedding chipfilm™ chips in polymers. Unlike the gluing process, embedding would be more realistic and more compatible with flexible systems. Different problems associated to gluing such as the realization of electrical contacts can be easily resolved by embedding the chips in polymers [8]. In this section we have examined the common embedding techniques and technology directions stated in different literature works. Later we shall elaborate the embedding process technology accomplished by us. Also we describe the delamination process and experiments performed to define the optimum polymer thickness.

A. Common Embedding Techniques
Variety of Polymers has been used for passivation, lamination and protection of the chip surface after wire bonding and contact making inside chip packages. Also for molding the chips inside packages, polymers are good candidates as they are very stable after thermal curing, highly flexible in nature and also have insulating properties. For the same reasons, researchers have chosen polyimides for embedding ultra-thin chips. The main demerits of polyimides are their high processing temperature, high thermal expansion coefficient compared to silicon, high water uptake and high outgassing during curing which have make the processing quite difficult [7].

To overcome these difficulties, polyimides with low thermal expansion co-efficient has been used for embedding Purpose. In this regard, several drying steps are conducted before each subsequent processing step during embedding process to avoid the water absorbed inside polyimides. The ultra-thin chips are adhered to the polyimide layer by means of BCB (Benzocyclobutene); a widely used polymer as dielectric material in microelectronic processing as polyimides have very poor adhesion to silicon [8-11].

B. Two Polymer Embedding Procedure
For our embedding purpose we have chosen the polyimide embedding technique over the low temperature one as we have opted for interconnect technology which involves much higher temperatures (in range of 300° - 400°C) and comparably smaller thickness then the mentioned system. In this regard we have started out experiments and testing with BCB and tried to imbed bare chips inside BCB. BCB resin is the dielectric material of choice in microelectronic industry because of its low dielectric constant, low moisture uptake, low curing temperature, high degree of planarization, good thermal stability and excellent chemical resistance.

The basic idea of the embedding is depicted in Fig. 2 where two different polymers are used for the complete process. Here, a polished silicon wafer or a glass substrate can be used as handling substrate. A removable adhesive is coated prior to the subsequent polymer coating for chip embedding so that the complete embedded chip stack can be delaminated after final the embedding process step. One of the polymers which is this case is BCB would be used for the embedding and realization of interconnects on the chips. The other Polymer is being used as the reinforcement layer on top and bottom of the stack which will hold the complete embedded chip system inside like a sandwich. In this regard, the reinforcement polymer should be highly flexible, non-fragile and at the same time stable and reliable so that it can hold the chip along with the complete stack inside. Examining the characteristics of different material, polyimides has been chosen as the reinforcement polymers for the embedding purpose. The metal contacts from the metal pads can be realized by means of
sputtering process. The possibility to etch Photo sensitive BCB and the ability of dry etching the polymer, makes the via opening task possible.

![Diagram](image)

Fig. 2. Two polymer ultra-thin chip embedding system

The two polymer embedding system has several advantages over the conventional single polyimide embedding technique mentioned in previous section. The single polyimide embedding system requires polyimides which has lower thermal expansion coefficient to avoid high shrinkage during chip embedding which can eventually introduce a mismatch between the chip and the polyimide. Moreover, low adhesion to silicon would hamper the long-term usage of the flexible system as excessive bending would deteriorate the chip-polyimide interfaces and might lead to chip displacement or delamination. High moisture uptake property of polyimide might also deteriorate the performance of the flexible system in long run.

Contrarily, embedding chips inside BCB would diminish the problem of high surface mismatch as well as the adhesion problem to the chip. As BCB has very low moisture uptake property (< 0.2%) and high planarization property, it can be a good preference for constructing flexible systems. Additionally, compatibility of BCB with different metals would make the realization of interconnects much easier and stable. But, because of fragile nature of BCB after curing, it cannot be used solely for embedding purpose. Hence, the two polymer embedding system could be a practical solution where two polyimide layers on top and bottom will provide the strength and flexibility to the embedded chip inside BCB.

The process flow of embedding ultra-thin chips by using two different polymers is elaborated in Fig. 3. At first, a special type of removable adhesive is spin coated on a blank polished silicon wafer used as handling carrier for the process. The first reinforcement polyimide layer is coated on top of the removal adhesive. The wafer has to be cured at 250°C temperature for about 2 hours so that the polyimide layer is completely dehydrated and the solvents are evaporated. In case of failing to evaporate the solvent and water from the layer prior to the subsequent spin coating, it can lead to creation of voids and delamination of the layers.

In the next step, the wafer is coated with BCB and cavities for chip placement are created on the BCB surface by means of contact lithography and subsequent development step. After curing the BCB layer, a second BCB layer is spun on the wafer and patterned to make the adhesive layer inside the cavity for chip placement. Then, the chips are placed immediately inside the cavity and pressed on the adhesive BCB layer. Our experiences have shown that this is the most critical part of the work as accurate chip placement and pressing needs much accuracy which cannot be achieved by means of manual placement. Rather a better and much precise automatic or semiautomatic tool has to be used. Failing to do that will introduce cavities under the chip or in much severe cases unwanted delamination of the chip can occur (Fig. 4-b). After the successful placement and bonding the chip, BCB is spun on to completely embed the chip inside and fill the cavities around it. The next step is the process of via opening on the desired contact pads for realization of interconnects. After the metallization process and metal etching, the complete area is covered with BCB again for planarization and protection of metal interconnects. Finally another polyimide layer is spun on the surface to completely embed the chip-BCB stack. The final openings are made on the polyimide layer to make the outside contact pads on the packaged chip.
We have successfully performed the embedding process and the complete embedded chip has been delaminated from the carrier surface. Although we have performed some successful metallization process on the polymers for experimental purpose, we are now trying to realize the process described in the previous paragraph regarding the metallization of the embedded chips.

C. Delamination Process

Delamination of the embedded system after the completion of the processing is one of the most important tasks to be addressed in case of ultra-thin chip embedding techniques. For this work we have carried out several experiments among which usage of perforated carrier process and the process of using an adhesion lowering coating was the most successful. They are described in details below.

1) Perforated Carrier process

For the realization of delamination method we have achieved limited success by using the perforated carrier process. In this process a perforated silicon wafer carrier has been used as handling substrate. A circular area of diameter 12 cm on the surface of a 15 cm silicon wafer was perforated through with 200 µm diameter holes and a pitch of 500 µm between the consecutive holes. The perforation of the carrier will allow the solvent to reach the adhesive layer underneath the embedded stack through the back side of the silicon substrate. We have selected a special type of removable adhesive from “DOW chemical company” and spin coated the polymer on the perforated carrier prior to the coating of the reinforcement polyimide layer and the subsequent polymer layers. The same process steps as depicted in Fig. 2 have been carried out. After completion of the embedding process on the carrier, the complete stack has been submerged in NMP (N-Methyl-2-pyrrolidone) for dissolving the removable adhesive. The solvent has been heated up to 70°C and the complete stack was submerged in the solvent for about 2 hours. The very first results from the experiment were positive as the solvent has dissolved the removable adhesive completely within an hour time. The main difficulty arises with the reinforcement polyimide which becomes unstable and partially dissolved in the solvent along with the removable adhesive, thus making the sandwich top and bottom layers to be unstable. Keeping the stack for a long time submerged in the solvent, results in dissolving the entire polyimide layer and the adhesive layer. The BCB layer along with the embedded chip was left alone floating in the solvent as BCB layer after curing becomes stable and resistant to chemicals. Although the main objective of the experiment was fulfilled by delamination of the stack, the released embedded chip stack becomes fragile because there was no reinforcement polyimide layers on both sides of BCB layer to provide stiffness and flexibility to the stack. A picture of the delaminated embedded chip is shown in Fig. 5-a. The cracks on the surface are due to the fragile nature of BCB and the dots on the surface are resulting from the perforation of the carrier.

2) Adhesion lowering process

Although we have achieved partial success with the perforated carrier process, it cannot be used for the delamination of the embedded stack as the process dissolves the polyimide layer. An alternative process is using an adhesion lowering layer which can reduce the adhesion of polyimide to the silicon. The adhesion lowering layer reduces the adhesion so that the polyimide layer sticks with very low force which is enough to keep the stack stable during subsequent processing step, yet very small force is needed to delaminate the stack from the carrier at the end of the process.

For this process we have spun on a special type of solvent on the wafer substrate prior to the coating of polyimides and the subsequent polymer layers. This solvent layer reduced the normal adhesion force of polyimide to the silicon and allows the polyimide layer to be delaminated from the carrier afterwards. This process introduced some difficulties regarding the adhesion of polyimide on the edge of the wafer. To overcome the problem, we have coated a ring shape BCB at the very edge of the wafer outside the chip embedding area prior to the polyimide coating. This process leads to a successful and smooth polyimide coating on the substrate without any delamination of polyimide layer. A picture of a delaminated embedded chip is shown in Fig. 5-b. Both surfaces of the stack appear to be very smooth and the complete piece is highly flexible and stable. The slight warpage effect of the piece is due to the thickness difference of polyimide on top and bottom of the stack. This issue will be discussed in the next section.

Fig. 4. SEM images of embedded ultra-thin chips inside BCB; a) successful embedding and b) failed embedding resulting from placement problems.

Fig. 5. Embedded ultra-thin chips inside polymers; a) delamination using perforated carrier process. Carrier perforation results in surface roughness on one side; b) delamination using adhesion lowering process. Both surfaces are very much smooth and the complete stack is highly conformable.
D. Optimization of Polymer Thickness

Polyimide has a high coefficient of thermal expansion (CTE) in the range of $55 \times 10^6 /{ }^\circ C$ which leads to very high expansion of the layer during thermal curing. When the polyimide layer is cooled down to the room temperature after curing, the polyimide tries to shrink again and eventually introduces a high stress situation at the interface where it is attached with a different material. In case of embedding ultra-thin chips inside polyimide, the CTE mismatch between silicon ($2.6 \times 10^6 /{ }^\circ C$) and the polyimide results in a high stress situation at the interface which can turn out to be fatal for the normal operation of the circuitry on the chip surface. This situation can also lead to unwanted delamination and imposed warpage effect on the chip. To avoid this problem either a low CTE polyimide has to be used for embedding chip or a different material which has a lower thermal expansion must be used.

As we have discussed before, in our case we have used BCB as the embedding polymer to avoid this problem. But due to the fragile nature of BCB after curing, high CTE polyimide layers has been placed on both sides of the embedded chip to provide the conformability and strength to the stack. We have performed several investigations to optimize the thickness of the polyimide. The thickness of the polymers used for embedding should be selected in a way so that on one hand, the polymer stack does not become fragile due to the high thickness of BCB and on the other hand the stack does not become so bulky that the flexibility is reduced drastically. The optimum thickness of the polyimide and the BCB layer was calculated in the range of 20-30 µm. In this regard, the polyimide layer on both sides has to be precisely controlled so that very small thickness mismatch is present to avoid inherent warpage effect resulting from high expansion of the polyimide layer. This effect is nicely depicted in Fig. 6 where a gradual increase of polyimide thickness on top of the embedded chip stack is shown.

![Fig. 6. Decrease of inherent warpage effect on polymers by controlling the deposited polymer thickness. Gradual increase in thickness from a) No polyimide on top and b) one thin layer of polyimide result in high warpage. The warpage effect is reduced by c) increasing the thickness on both side and d) almost equal thickness of polymide on both sides diminishes the warpage.](image)

IV. ULTRA-THIN CHIP WARPAGE

Due to high conformability of ultra-thin chips, they are good candidate for being used in flexible electronics technologies. While this flexible nature of ultra-thin chips is an advantage for diverse applications, it can also bring forth new challenges for the construction of interconnect technology. Due to very low thickness of ultra-thin chips, mechanical stress mismatches are introduced between different layers in the chip which eventually lead to significant deformation of the chips[6, 12]. This deformation also known as warpage can lead to difficulties during the chips are embedded inside polymers and therefore need to be minimized. For minimizing the warpage effect it is necessary to determine the possible sources that lead to the warpage effect and then to optimize the manufacturing process accordingly to diminish or reduce the warpage effect. In Fig. 7-a, the surface profile of a Chipfilm™ chip (thickness of approx. 18 µm) prior to the circuit integration is shown. This chip has only a very small warpage resulting from the 16 µm epitaxial layer on a porous layer of approx. 2 µm (Fig. 1). Contrary to that, Fig. 7-b is showing a relatively high warpage effect on the surface profile of the similar type Chipfilm™ chip with only 0.2 µm thermal oxide layer deposited on top. Although the difference of the thickness in only a fraction of a micron, a higher warpage effect can be observed on the second chip. This difference in the warpage effect can be attributed to high CTE mismatch between the silicon ($2.6 \times 10^6 /{ }^\circ C$) and silicon dioxide (0.5x$10^6 /{ }^\circ C$) and eventually to high temperature oxidation process.

![Fig. 7. Surface profile of ultra-thin Chipfilm™ chips; a) before circuit integration and b) with a protective oxide layer on top](image)

In addition to this, different steps during further processing of the chip such as metallization and deposition of passivation layer can add up to inherent warpage effect of the chip. Recently we have shown that the degree and shape of the warpage effect primarily depends on the chip layout and surface topology [6].

A. Effect of chip warpage on embedding

Chip warpage has a profound effect on the embedding of ultra-thin chips. It can lead to unwanted void formation under the chip, displacement and even unlikely delamination of the chip from the polymer surface (Fig. 4). Warpage effect can also create problems during lithography and metallization steps. Even a void free placement of warped ultra-thin chip can lead to deformation after the delamination of embedded chip stack. For this reason the warpage effect has to be completely avoided by introducing controlled process steps and deposition of stress neutralizing layers on highly warped chips.

V. FUTURE AIMS

Although the primary ultra-thin chip embedding process was roughly successful with some minor imperfections, the process has to be further improved. Several challenges such as accurate chip placement, polyimide thickness optimization and
chip warpage have to be resolved during our future advancements to achieve a reliable and efficient chip embedding process. One of the most important tasks is the realization of external interconnects on the embedded chip. Several primary experiments have been successfully done to investigate the compatibility of metallization process with the polymers. Now we need to realize the metallization process on embedded chips directly. One of the main aims after successful embedding and metallization process is to adapt the process to a complete industrialized process. This will allow the process to be successfully implemented in the future chip production lines and for realization of low cost high reliability system integration.

VI. Conclusion

In this paper we have presented our first results on embedding ultra-thin Chipfilm™ chips inside polyimide. In this regard, we have discussed the two polymer embedding technique where one of the polymers is used for embedding the chip and the other as the reinforcement layer on top and bottom of the embedded stack. The embedding of ultra-thin chips has been successfully performed by using the two polymer technique and has been demonstrated in this paper. We have also elaborated two delicate delamination processes for releasing the complete embedded chip stack from the substrate. In our future works we are going to improve the embedding process further by overcoming the complications that we have discussed in this paper to reach an optimized process. We would also extend the work to achieve further improvements with embedding process. Additionally, we would work for developments of metallization process on embedded chip to realize an optimized interconnect technology.

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