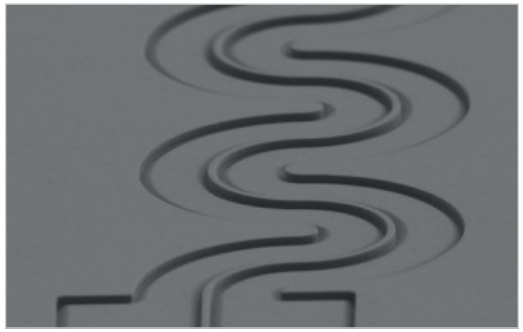
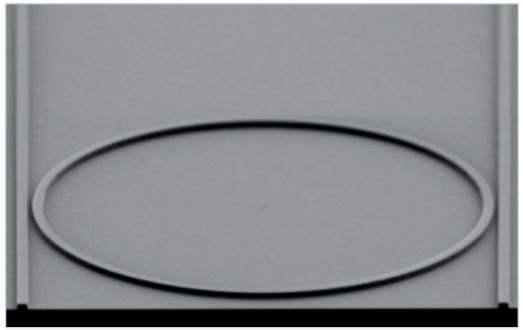
PASSIVE DEVICES

Passive devices cover the coupling the light in and out the chip, the waveguide circuit on the chip and the covering material. The process consists typically of two silicon etching steps patterning the grating couplers and the waveguides. A low temperature oxide (TEOS) protects the patterned photonic structures. Patterning of the oxide as well as additional process steps are possible.



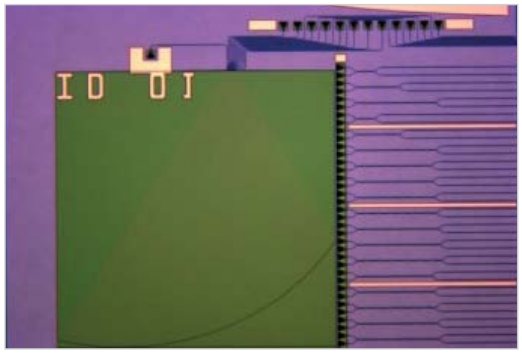


Process example: Passive device

Silicon patterning 1	70 nm etch
Silicon patterning 2	220 nm full etch
Oxide deposition	1 µm

MIX AND MATCH LITHOGRAPHY

The mix and match approach upgrades the process of active devices with the free choice of our lithography tools.



Process example: Mix and match lithography

Implant 1	i-line stepper
Implant 2	i-line stepper
Silicon patterning 1	e-beam
Silicon patterning 2	e-beam
Silicon patterning 3	i-line stepper
Oxide patterning 1	e-beam
Oxide patterning 2	e-beam
Metal 1	laser direct writer

Contact

ims chips
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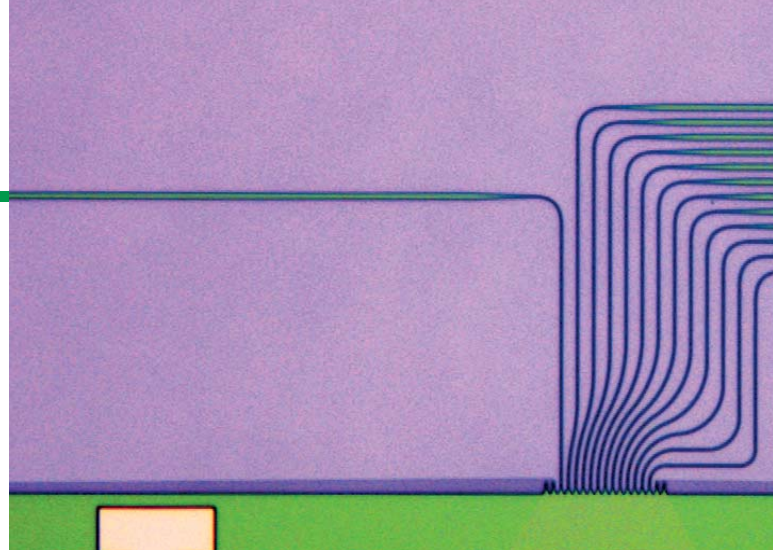
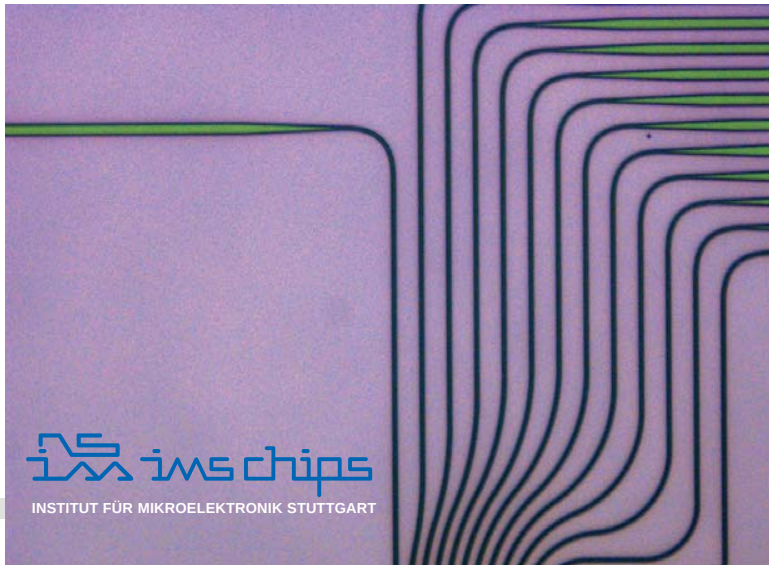


Silicon Photonics

New technology started:
Passive devices, Active devices, Mix and Match Lithography



ims chips
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NEW TECHNOLOGY STARTED

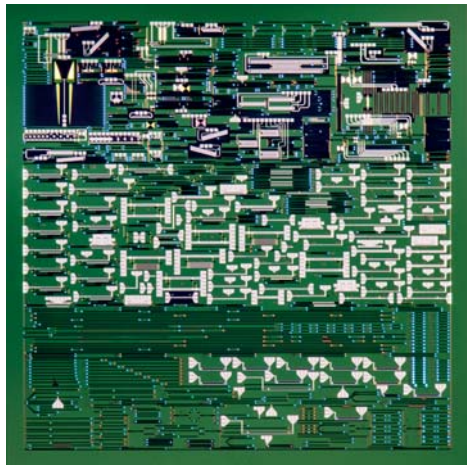
Passive devices, Active devices, Mix and Match Lithography

Silicon Photonics is going to revolutionize the market data communication circuits and integrated sensor technology. IMS has established technology lines for passive and active optical circuits and devices. Exemplary processes are shown on the next pages. All Silicon Photonic chips are completely fabricated in-house including assembly and packaging.

Dependent on the customers demand IMS can provide mix and match lithography: our state of the art variable e-beam system is capable of patterning complex arbitrary designs with high resolution. For lower resolution a cost-effective i-line stepper can be used. A direct laser writing tool enables rapid prototyping. All lithography techniques can be combined in one process flow with multiple layers.

The devices are typically fabricated on 6" (150 nm) SOI substrates using CMOS and MEMS technologies. More than 20 years of experiences on etching, epitaxy and ion implantation will help to reach your desired process specifications.

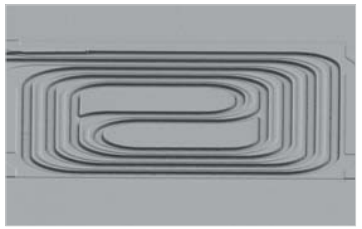
PROCESS SPECIFICATIONS



Substrate size	150 mm (6 inch)
Substrate type	Silicon bulk SOI
SOI type Active Layer (typical) Buried Oxide (typical)	 220 nm - 260 nm 2 µm – 3 µm
Chip size I-line lithography E-beam writing Direct laser writing	 up to 17 mm x 22 mm up to substrate size up to substrate size
Waveguide losses at 1550nm (waveguide width: 400 nm)	TE-mode: < 5dB/cm TM-mode: < 3dB/cm
Slot lines in silicon Width Etching depth	 60 nm 250 nm
Typical Packaging	1 cm^2 chips dicing

ACTIVE DEVICES

Active devices allow the manipulation of the optical signals with electrical parameters leading to modulators, interferometers or filters. This process features considerably more steps as different doping levels and metal contacts are required. We provide a completely CMOS-compatible process with the possibility of additional process steps as backside patterning using MEMS-technology and inert metal contacts for assembly.



Process example: Active device

Implant 1	low n-type 10^{16} cm^{-3}
Implant 2	high n-type 10^{19} cm^{-3}
Implant 3	low p-type 10^{16} cm^{-3}
Implant 4	high p-type 10^{19} cm^{-3}
Silicon patterning 1	70 nm etch
Silicon patterning 2	180 nm etch
Silicon patterning 3	250 nm full etch
Oxide deposition	1 um
Oxide patterning	1 um etch
Metal 1	500 nm AlSiCu
Metal 2	200 nm Cr/Au
Backside structuring	Membrane etch to BOX
Metal 3 backside	200 nm Al